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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/008,700 | 12/07/2001 | Hong-Sik Jeong | 5649-905 | 5150 |

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MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

| EXAMINER | |
|---|---|
| LUU, CHUONG A | |
| **ART UNIT** | **PAPER NUMBER** |
| 2825 | |

DATE MAILED: 04/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/008,700 | JEONG ET AL. | |
| | Examiner | Art Unit | |
| | Chuong A Luu | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Inventorship*

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

## PRIOR ART REJECTIONS

### Statutory Basis

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**The Rejections**

Claims 1 and 3-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Lur et al. (U.S. 6,013,569)

Lur discloses one-step salicide process without bridging by

**(1)** forming an insulating layer (52) on a substrate (50);

forming a capping layer (54) on the insulating layer (52);

patterning the capping layer and the insulating layer;

forming insulating spacers (58) on sidewalls of the insulating layer (52) such that the insulating layer (52) is enclosed by the insulating spacers (58), the capping layer (54), and the substrate (50);

**(3)** wherein the capping layer may comprise at least one of silicon oxide, silicon nitride, undoped polysilicon, doped polysilicon, or $Al_2O_3$ (see column 6, lines 63-65);

**(4)** wherein the insulating layer is a first insulating layer, and wherein forming the insulating spacers comprises: forming a second insulating layer on the capping layer, the sidewalls of the first insulating layer, and the substrate; and etching the second insulating layer so as to expose the substrate and an upper surface of the capping layer, opposite the substrate (see Figures 5-8);

Claims 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. (U.S. 6,013,569)

Lur discloses the claimed invention except for wherein each of the insulating spacers has a width in a range of about 300Å to about 500Å (see column 7, lines 40-65). It would have been obvious to one of that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 and In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 6-9, 12-20 and 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weybright et al. (U.S. 6,548,357 B2) in view of Lur et al. (U.S. 6,013,569)

Weybright discloses a process for optimized definition of array and logic devices with

**(6); (15); (25)** forming a pattern comprising a pair of mesa regions on a substrate (10) (see Figure 7);

forming a first insulating layer (30) on the pair of mesa regions (see Figure 8);

forming a second insulating layer (32) on the pair of mesa regions and the substrate (10) (see Figure 9);

**(7); (16); (28)** wherein the second insulating layer is a spin on glass layer;

**(14); (23)** wherein each of the insulating spacers has a width in a range of about 50Å to about 200Å (see column 8, lines 10-14);

**(18)** further comprising: removing at least a portion of the etch stop layer from a contact region between the pair of mesa regions;

**(27)** further comprising: forming a contact pad on the substrate that is self aligned by the gate electrode;

Weybright teaches the above outlined features except for forming a capping layer on the second insulating layer; patterning the capping layer and the second insulating layer; forming insulating spacers on sidewalls of the second insulating layer such that the second insulating layer is enclosed by the insulating spacers, the capping layer, the first insulating layer, and the substrate. However, Lur discloses one-step salicide process without bridging by **(1); (15); (25)**....forming a capping layer on the second insulating layer; patterning the capping layer and the second insulating layer; forming insulating spacers on sidewalls of the second insulating layer such that the second insulating layer is enclosed by the insulating spacers, the capping layer, the first insulating layer, and the substrate (see Figures 5-8); **(8); (19)** further comprising: applying a cleaning solution to the integrated circuit device so as to expose a contact region between the pair of mesa regions by removing at least a portion of a native oxide layer from the contact region; **(9); (20)** wherein the cleaning solution comprises at least one of hydrofluoric (HF) acid or a mixture of $NH_4OH$, $H_2O_2$, and $H_2O$ (see columns 9 and 10, lines 33-67 and lines 1-10, respectively); **(12); (24)** wherein the capping layer may comprise at least one of silicon oxide, silicon nitride, undoped polysilicon, doped polysilicon, or $Al_2O_3$ (see column 6, lines 63-65); **(13)** wherein forming the insulating spacers comprises: forming a third insulating layer on the capping layer, the sidewalls of

the second insulating layer, and the substrate; and etching the third insulating layer so as to remove at least a portion of the third insulating layer from the substrate and an upper surface of the capping layer, opposite the substrate; **(17)** wherein forming the insulating spacers comprises: forming a third insulating layer on the capping layer, the sidewalls of the second insulating layer, and the etch stop layer; and etching the third insulating layer so as to remove at least a portion of the third insulating layer from the second insulating layer and an upper surface of the capping layer, opposite the substrate; **(26)** wherein forming the protective layer comprises: forming a capping layer on an upper surface of the second insulating layer, opposite the substrate; and forming insulating spacers on sidewalls of the second insulating layer (see Figures 5-8). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to combine the above teachings of Weybright and Lur to manufacture a semiconductor device to exceed its performance criteria

Claims 10-11 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weybright et al. (U.S. 6,548,357 B2) in view of Lur et al. (U.S. 6,013,569) and further in view of Huang (U.S. 6,489,230 B1)

Weybright and Lur teaches everything above except for further comprising: forming a conductive layer on the pair of mesa regions and the substrate so as to fill a contact region between the pair of mesa regions and to cover the mesa regions; removing a portion of the conductive layer such that an upper surface of the first insulating layer, opposite the substrate, is exposed; wherein removing the portion of the

conductive layer comprises: chemical mechanical polishing the conductive layer such that the upper surface of the first insulating layer, opposite the substrate, is exposed. Furthermore, Huang discloses a semiconductor device with **(10); (21)** further comprising: forming a conductive layer on the pair of mesa regions and the substrate so as to fill a contact region between the pair of mesa regions and to cover the mesa regions; removing a portion of the conductive layer such that an upper surface of the first insulating layer, opposite the substrate, is exposed (see Figures 1F and 1H); **(11); (22)** wherein removing the portion of the conductive layer comprises: chemical mechanical polishing the conductive layer such that the upper surface of the first insulating layer, opposite the substrate, is exposed (see column 6, lines 26-50). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to combine the above teachings Weybright, Lur and Huang to fabricate a semiconductor device to exceed its performance criteria.

## *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Weybright, Lur and Huang disclose a method of forming a semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (703)305-0129. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

CAL

CAL
April 21, 2003

C. Everhart
CARIDAD EVERHART
PRIMARY EXAMINER